ABSTRACT OF DISCLOSURE

A three-dimensional (3-D) integrated chip system is provided with a first wafer including one or more integrated circuit (IC) devices, metallic lines deposited via an interlevel dielectric (ILD) on a surface, and at least one barrier line deposited on an outer edge of the surface; and a second wafer including one or more integrated circuit (IC) devices, metallic lines deposited via an interlevel dielectric (ILD) on a surface, and at least one barrier line deposited on an outer edge of the surface, wherein the metallic lines and the barrier line deposited on the surface of the second wafer are bonded with the metallic lines and the barrier line deposited on the surface of the first wafer to establish electrical connections between active IC devices on adjacent wafers and to form a barrier structure on the outer edge of the adjacent wafers.